

PX-CBL-IR4-40G-QSFP-2KM-A

40GBASE, QSFP+ IR4, (SM)

1260 NM - 1555 NM, 2 KM REACH, MTP/MPO

PX-CBL-IR4-40G-QSFP-2KM-A

40GBASE, QSFP+ IR4 Transceiver

Features

- 4 Parallel lanes design
- Up to 11.2Gb/s data rate per channel
- Aggregate Bandwidth of up to 44.0G
- QSFP+ MSA compliant
- Up to 2km transmission on single mode fiber (SMF)
- Maximum power consumption 3.5W
- Single +3.3V power supply
- Operating case temperature: 0~70°C
- RoHS-6 compliant



Applications

- 40G Ethernet
- Infiniband QDR, DDR and SDR
- Datacenter and Enterprise networking

1. General Description

This product is a parallel 40Gb/s Quad Small Form-factor Pluggable (QSFP+) optical module. It provides increased port density and total system cost savings. The QSFP+ full-duplex optical module offers 4 independent transmit and receive channels, each capable of 10Gb/s operation for an aggregate data rate of 40Gb/s on 1.4km of single mode fiber.

An optical fiber ribbon cable with an MTP/MPO connector can be plugged into the QSFP+ module receptacle. Proper alignment is ensured by the guide pins inside the receptacle. The cable usually cannot be twisted for proper channel to channel alignment. Electrical connection is achieved through a z-pluggable 38-pin connector per MSA requirement.

The module operates with single +3.3V power supply. LVCMOS/LVTTL global control signals, such as Module Present, Reset, Interrupt and Low Power Mode, are available with the modules. A 2-wire serial interface is available to send and receive more complex control signals, and to receive digital diagnostic information. Individual channels can be addressed and unused channels can be shut down for maximum design flexibility.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external

operating conditions including temperature, humidity and EMI interference. The module can be managed through the I2C two-wire serial interface.

2. Functional Description

This product is a QSFP+ parallel single mode optical transceiver with an MTP/MPO fiber ribbon connector. The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also voltage compatible with Common Mode Logic (CML) levels. All data signals are differential and support a data rates up to 10.3Gb/s per channel. Figure 1 shows the functional block diagram of this product.

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. Per MSA the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL.

Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP+ modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP+ module must be used.

Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP+ memory map.

The ResetL pin enables a complete module reset, returning module settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.

Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulled up to the host Vcc. When a module is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. Low indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

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3. Transceiver Block Diagram

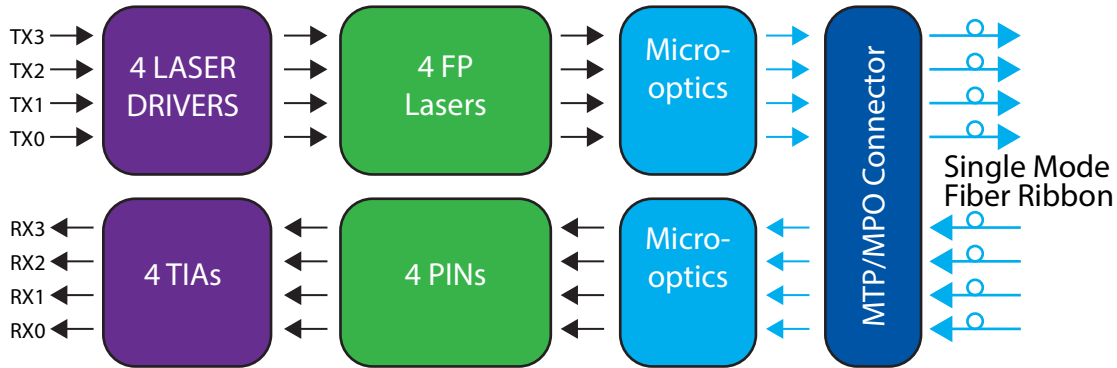


Figure 1. Transceiver Block Diagram

4. Pin Assignment and Pin Description

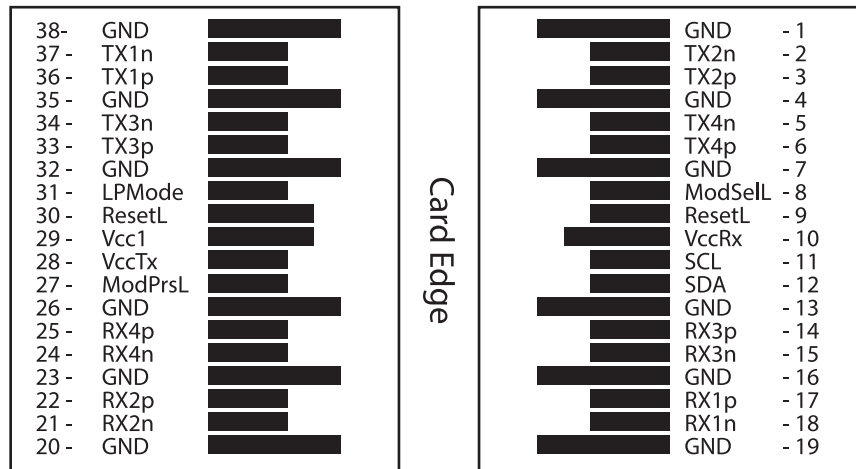


Figure 2. MSA compliant Connector

5. Pin Definition

PIN	Logic	Symbol	Name/Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSelL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVC MOS-I/O	SCL	2-Wire Serial Interface Clock	

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PIN	Logic	Symbol	Name/Description	Notes
12	LVC MOS-I/O	SDA	2-Wire Serial Interface Data	
13		GND	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	1
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3 V Power Supply transmitter	2
30		Vcc1	+3.3 V Power Supply	2
31	LVTTL-I	LPMODE	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP+ modules. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 and Vcc Tx may be internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

6. Recommended Power Supply Filter

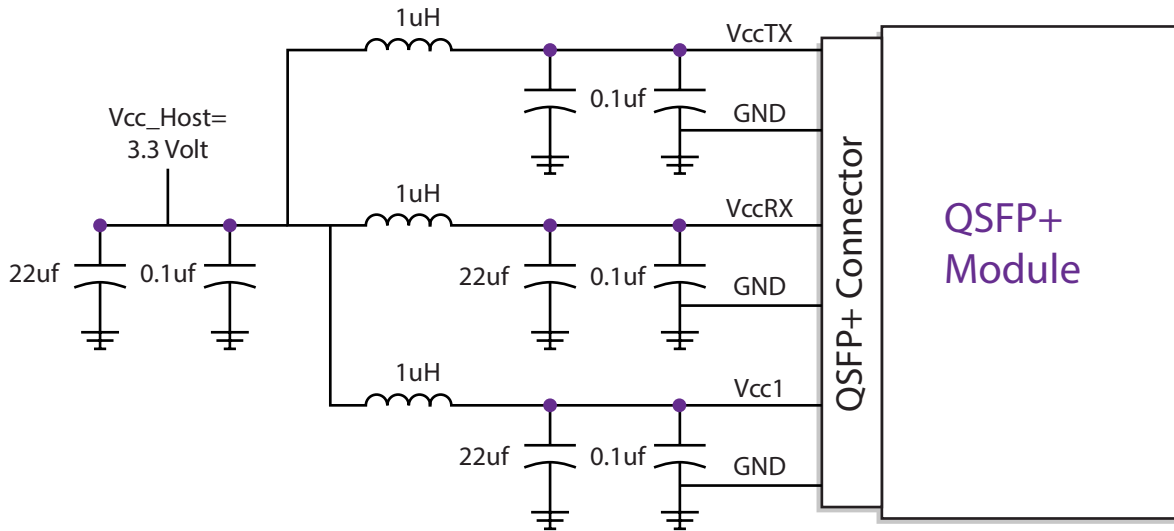


Figure 3. Recommended Power Supply Filter

7. Absolute Maximum Ratings

It has to be noted that the operation in excess of any individual absolute maximum ratings might cause permanent damage to this module.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	TS	-40	85	°C	
Operating Case Temperature	TOP	0	70	°C	
Power Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	
Damage Threshold, each Lane	THd	3.3		dBm	

8. Recommended Operating Conditions and Power Supply Requirements

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	TOP	0		70	°C
Power Supply Voltage	VCC	3.135	3.3	3.465	V
Data Rate, each Lane			10.3125	11.2	Gb/s
Control Input Voltage High		2		Vcc	V
Control Input Voltage Low		0		0.8	V
Link Distance with G652	D			1.4	km

9. Electrical Characteristics

The following electrical characteristics are defined over the Recommended Operating Environment unless otherwise specified.

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Power Consumption				3.5	W	
Supply Current	I _{cc}			1.1	A	
Transceiver Power-on Initialization Time			2000	ms	1	
Transmitter (each Lane)						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Single-ended Input Voltage Tolerance (Note 2)		-0.3		4.0	V	V Referred to TP1 signal common
AC Common Mode Input Voltage Tolerance (RMS)		15			mV	
Differential Input Voltage Swing Threshold		50			mV _{pp}	LOSA Threshold
Differential Input Voltage Swing	V _{in,pp}	190		700	mV _{pp}	
Differential Input Impedance	Z _{in}	90	100	110	Ω	
Differential Input Return Loss		See IEEE 802.3ba 86A.4.11			dB	10MHz-11.1GHz
J2 Jitter Tolerance	J _{t2}	0.17			UI	
J9 Jitter Tolerance	J _{t9}	0.29			UI	
Data Dependent Pulse Width Shrinkage (DDPWS) Tolerance		0.07			UI	
Eye Mask Coordinates {X1, X2 Y1, Y2}		0.11, 0.31 95, 350			UI _{mV}	Hit Ratio = 5x10 ⁻⁵
Receiver (each Lane)						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Single-ended Output Voltage		-0.3		4.0	V	Referred to signal common
AC Common Mode Output Voltage (RMS)				7.5	mV	
Differential Output Voltage Swing	V _{out,pp}	300		850	mV _{pp}	
Differential Output Impedance	Z _{out}	90	100	110	ohm	

Receiver (each Lane)						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Termination Mismatch at 1MHz				5	%	
Differential Output Return Loss		See IEEE 802.3ba 86A.4.2.1			dB	10MHz-11.1GHz
Common Mode Output Return Loss		See IEEE 802.3ba 86A.4.2.2			dB	10MHz-11.1GHz
Output Transition Time		28			ps	20% to 80%
J2 Jitter Output	Jo2			0.42	UI	
J9 Jitter Output	Jo9			0.65	UI	
Eye Mask Coordinates {X1, X2 Y1, Y2}		0.29, 0.5 150, 425			UImV	Hit Ratio = 5x10 ⁻⁵

Notes:

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above the minimum recommended operating supply voltages to the time when the module is fully functional.
2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.

10. Optical Characteristics

All parameters are specified under the recommended operating conditions with PRBS31 data pattern unless otherwise specified.

Transmitter						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Center Wavelength	λ_C	1260	1310	1355	nm	
RMS Spectral Width	$\Delta\lambda_{rms}$			3.5	nm	
Average Launch Power, each Lane	PAVG	-6		1.5	dBm	1
Optical Modulation Amplitude (OMA), each Lane	POMA	-4.5		3.0	dBm	2
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			6.5	dB	
Launch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane	OMA-TDP	-5.5			dBm	
TDP, each Lane	TDP			3.2	dB	
Extinction Ratio	ER	3.5			dB	

Transmitter						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Relative Intensity Noise	RIN			-128	dB/Hz	
Optical Return Loss Tolerance	TOL			12	dB	
Transmitter Reflectance	RT			-12	dB	
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				
Receiver						
Parameter	Symbol	Min	Typical	Max	Unit	Notes
Center Wavelength	λ_C	1260	1310	1355	nm	
Damage Threshold, each Lane	THd	3.3			dBm	3
Average Power at Receiver Input, each Lane		-11.5		2.3	dBm	
Receiver Reflectance	RR			-12	dB	
Receiver Sensitivity in OMA, each Lane	SEN			-10.6	dBm	Informative
Difference in Receive Power between any Two Lanes (OMA)	Prx,diff			7.5	dB	
LOS Assert	LOSA	-30			dBm	
LOS Deassert LOSD			-15		dBm	
LOS Hysteresis	LOSH	0.5			dB	
Receiver Electrical 3 dB upper Cutoff Frequency, each Lane	Fc			12.3	GHz	

Notes:

1. The maximum transmitter average optical power of 1.5 dBm is well within the guardband of receiver overload specifications of commercially available 10GBASE-LR SFP+ transceivers offered by Approved Networks and other vendors.
2. Even if the TDP < 1 dB, the OMA min must exceed the minimum value specified here.
3. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical input signal having this power level on one lane. The receiver does not have to operate correctly at this input power.

11. Optical Characteristics

All parameters are specified under the recommended operating conditions with PRBS31 data pattern unless otherwise specified.

Parameter	Symbol	Min	Max	Unit	Notes
Temperature monitor absolute error	DMI_Temp	-3	3	°C	Over operating temperature
Supply voltage monitor absolute error	DMI_VCC	-0.1	0.1	V	Full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor DMI_Ibias_Ch	-10%	10%	mA		
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/- 1 dB fluctuation, or a +/- 3 dB total accuracy.

12. Mechanical Dimensions

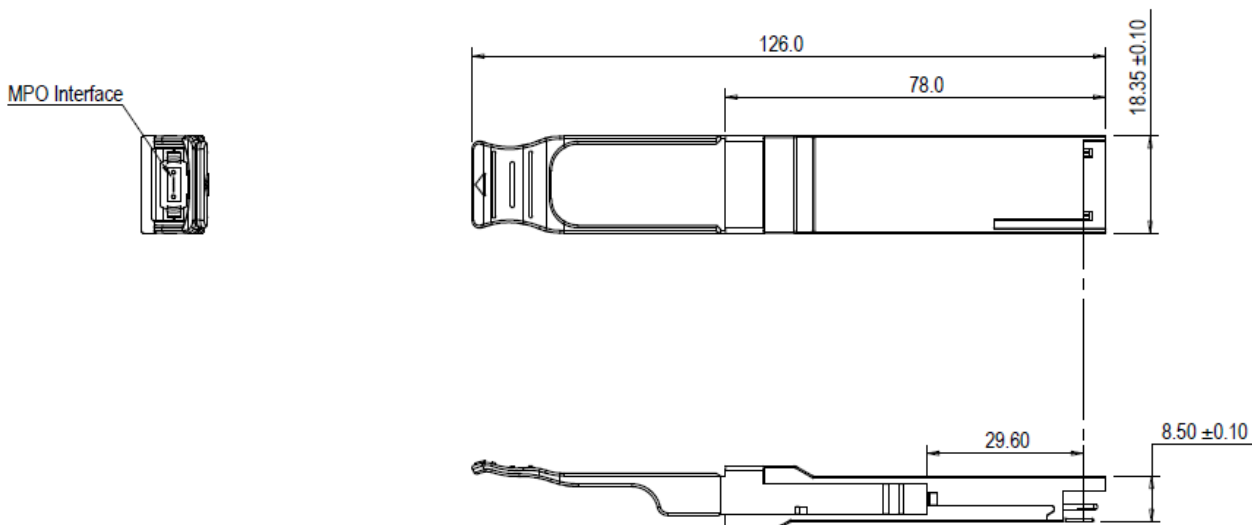


Figure 4. Mechanical Outline

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Attention:

To minimize MPO connection induced reflections, an MPO receptacle with 8-degree angled end-face is utilized for this product. A female MPO plug connector with 8-degree end-face should be used with this product as illustrated in Figure 5.

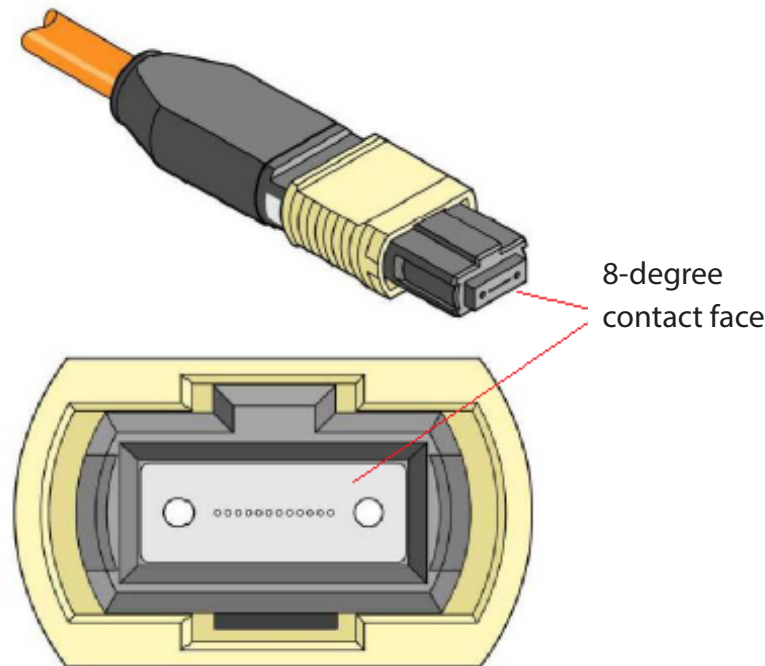


Figure 5. Female MPO Connector with 8-degree End-face

13. ESD

This transceiver is specified as ESD threshold 1KV for high speed data pins and 2KV for all others electrical input pins, tested per MIL-STD-883, Method 3015.4 /JESD22-A114-A (HBM). However, normal ESD precautions are still required during the handling of this module. This transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

14. Laser Safety

This is a Class 1 Laser Product according to IEC 60825-1:2007. This product complies with 21 CFR 1040.10 and 1040.11 except for deviations pursuant to Laser Notice No. 50, dated (June 24, 2007).

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15. Contact Information

Approved Networks is a leading supplier of Network Transceivers and Connectivity products to Channel Partners, Resellers, and OEMs. With more than 9 years of direct industry experience, our products are resident in the most demanding and mission critical functional networks Worldwide. We serve as a Master Distributor to the largest CMs in the world and deploy the most rigorous testing and firmware management programs to bring the highest level of functional product to the market at a cost that makes sense.

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