

J8438A-A
10GBASE, X2, ER Transceiver

Features

- Compatible with X2 MSA Rev2.0b
- Support of IEEE 802.3ae 10GBASE-ER at 10.3125Gbps
- Transmission Distance up to 40Km(SMF)
- SC Receptacle 1550nm Cooled EA-DFB Laser
- SC Duplex Optical Connector
- Hot Pluggable 70-PIN Connector with XAUI Electrical Interface
- Management and control via MDIO 2-wire interface
- Power Supply : +5V, +3.3V, APS(+1.2V)
- Diagnostic Optics Monitoring
- Temperature Range: 0~ 70 °C
- ROHS Compatible



Applications

- 10GE Ethernet switches and routers
- 10GE Core-routers
- 10GE Storage
- Other 10Gbps Ethernet Transmission System

1. Product Description

The J8438A-A is a highly integrated, Serial optical transponder module for high-speed, 10Gbit/s data transmission applications. 4x3.125Gbps Ethernet Signal Input by XAUI Interface. An integrated Coder / Decoder and multiplexer / demultiplexer (SERDES: Serializer / Deserializer). Designing for 40km Transmission with an uncooled directly modulated 1550nm Cooled EA-DFB Laser. Digital diagnostics functions are available via a 2-wire serial interface, as specified in the XENPAK MSA 3.0.

2. Absolute Maximum Ratings

Any stress beyond the maximum ratings can result in permanent damage. The device specifications are guaranteed only under the recommended operating conditions.

Parameter	Symbol	Min	Max	Unit	Notes
Storage Ambient Temperature Range		-40	+85	°C	non condensing
Powered case Temperature Range		0	+70	°C	non condensing
Adaptable Power Supply (APS)	Vapsense	0	1.5	V	Voltage @ Pin APS Sense
Supply Voltage Range @ 3.3V	Vcc3	-0.5	4.0	V	

2. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Operating Case Temperature	Tc	0		+70	°C
Power Supply Voltage	VCC5	4.75	5.0	5.25	V
	VCC3	3.14	3.3	3.47	
	VAPS	1.152	1.2	1.248	
Power Dissipation	PD			4	W

3. XAUI I/O Characteristics

Parameter	Symbol	Min	Typ.	Max	Unit	Note
XAUI Data Rate	DR		3.125		Gb/s	
XAUI Baud Rate Tolerance		-100		+100	ppm	Relative Tolerance
Differential Input Voltage Swing		220		1600	mv	8B/10B Coded Input Signal
Differential Output Voltage Swing		800		1600	mVp-p	RLOAD = 100Ω ± 5%
Differential Input Impedance		80	100	120	Ω	
Total Output Jitter	TJXAUI			0.35	UI	no pre-equalization
Total Deterministic Output Jitter	DJXAUI			0.17	UI	no pre-equalization

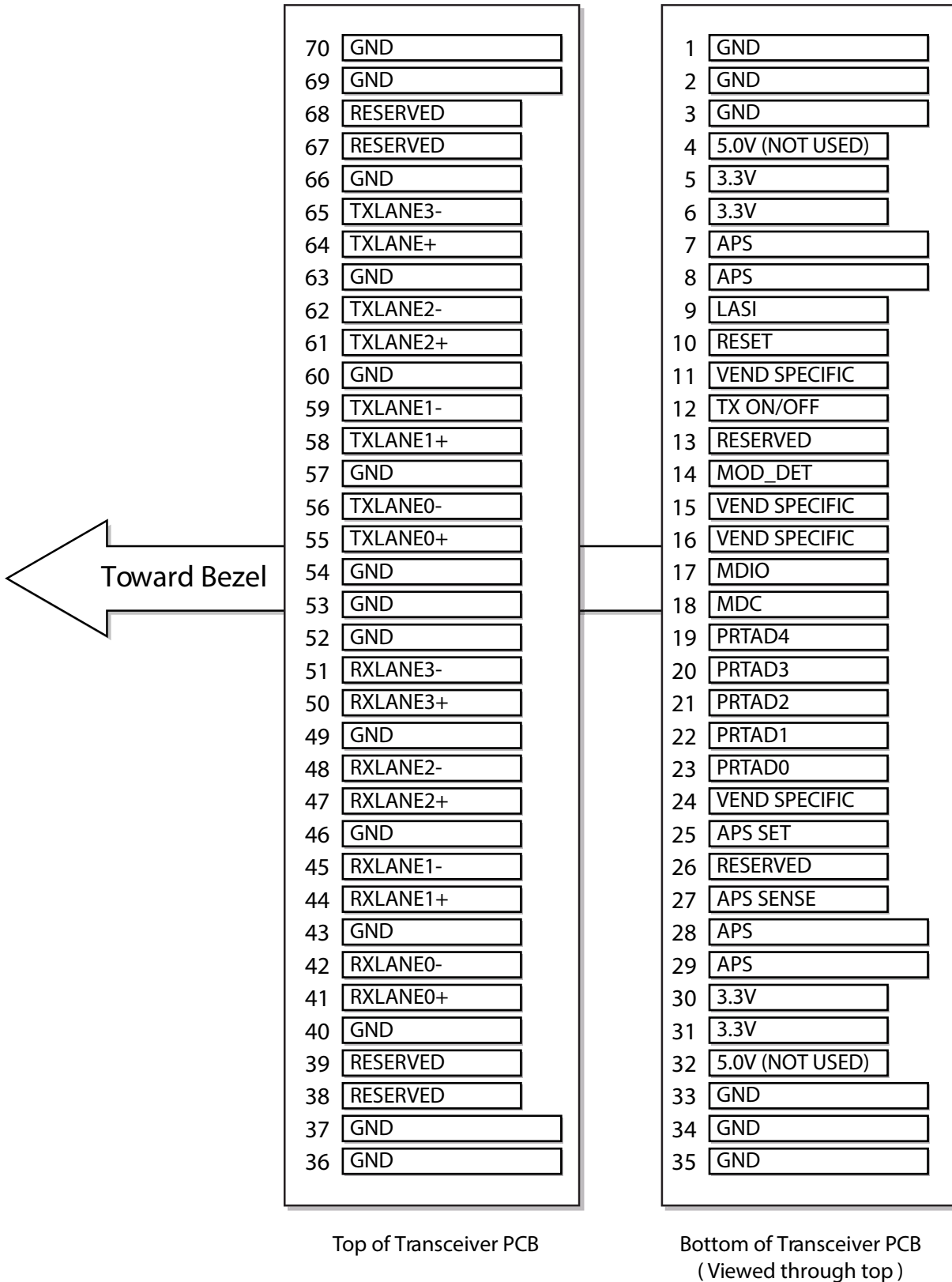
4. Optical Interface

Transmitter						
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Operating Range				40 Km		
Operating Date Rate			10.3125		Gb/s	
Optical Transmit Power	Po	-1.0		+2.0	dBm	
Input Centre Wavelength	λ	1530	1550	1570	nm	
SMSR	SWSR	30			dB	
Extinction Ratio	ER	9.0				
Optical Modulation Amplitude	OMA	500			μ W	
Transmitter and Dispersion Penalty	TDP			3.2	dB	
Receiver						
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Operating Date Rate			10.3125		Gb/s	
Overload	Po	0.5			dBm	
Sensitivity in 10.3G(OMA)	OMA0			-14.1	dBm	1
Stressed Sensitivity in 10.3G(OMA)	OMAst			-11.3	dBm	1

Notes:

1. Measured at 10.3125Gb/s,Non-framed PRBS2^31-1,NRZ

5. Electrical PAD Layout



6. Host PCB X2 PINOUT

1	<input type="checkbox"/>	GND	GND	<input type="checkbox"/>	70
2	<input type="checkbox"/>	GND	GND	<input type="checkbox"/>	69
3	<input type="checkbox"/>	GND	RESERVED	<input type="checkbox"/>	68
4	<input type="checkbox"/>	5.0V (NOT USED)	RESERVED	<input type="checkbox"/>	67
5	<input type="checkbox"/>	3.3V	GND	<input type="checkbox"/>	66
6	<input type="checkbox"/>	3.3V	TXLANE3-	<input type="checkbox"/>	65
7	<input type="checkbox"/>	APS	TXLANE+	<input type="checkbox"/>	64
8	<input type="checkbox"/>	APS	GND	<input type="checkbox"/>	63
9	<input type="checkbox"/>	LASI	TXLANE2-	<input type="checkbox"/>	62
10	<input type="checkbox"/>	RESET	TXLANE2+	<input type="checkbox"/>	61
11	<input type="checkbox"/>	VEND SPECIFIC	GND	<input type="checkbox"/>	60
12	<input type="checkbox"/>	TX ON/OFF	TXLANE1-	<input type="checkbox"/>	59
13	<input type="checkbox"/>	RESERVED	TXLANE1+	<input type="checkbox"/>	58
14	<input type="checkbox"/>	MOD_DET	GND	<input type="checkbox"/>	57
15	<input type="checkbox"/>	VEND SPECIFIC	TXLANE0-	<input type="checkbox"/>	56
16	<input type="checkbox"/>	VEND SPECIFIC	TXLANE0+	<input type="checkbox"/>	55
17	<input type="checkbox"/>	MDIO	GND	<input type="checkbox"/>	54
18	<input type="checkbox"/>	MDC	GND	<input type="checkbox"/>	53
19	<input type="checkbox"/>	PRTAD4	GND	<input type="checkbox"/>	52
20	<input type="checkbox"/>	PRTAD3	RXLANE3-	<input type="checkbox"/>	51
21	<input type="checkbox"/>	PRTAD2	RXLANE3+	<input type="checkbox"/>	50
22	<input type="checkbox"/>	PRTAD1	GND	<input type="checkbox"/>	49
23	<input type="checkbox"/>	PRTAD0	RXLANE2-	<input type="checkbox"/>	48
24	<input type="checkbox"/>	VEND SPECIFIC	RXLANE2+	<input type="checkbox"/>	47
25	<input type="checkbox"/>	APS SET	GND	<input type="checkbox"/>	46
26	<input type="checkbox"/>	RESERVED	RXLANE1-	<input type="checkbox"/>	45
27	<input type="checkbox"/>	APS SENSE	RXLANE1+	<input type="checkbox"/>	44
28	<input type="checkbox"/>	APS	GND	<input type="checkbox"/>	43
29	<input type="checkbox"/>	APS	RXLANE0-	<input type="checkbox"/>	42
30	<input type="checkbox"/>	3.3V	RXLANE0+	<input type="checkbox"/>	41
31	<input type="checkbox"/>	3.3V	GND	<input type="checkbox"/>	40
32	<input type="checkbox"/>	5.0V (NOT USED)	RESERVED	<input type="checkbox"/>	39
33	<input type="checkbox"/>	GND	RESERVED	<input type="checkbox"/>	38
34	<input type="checkbox"/>	GND	GND	<input type="checkbox"/>	37
35	<input type="checkbox"/>	GND	GND	<input type="checkbox"/>	36

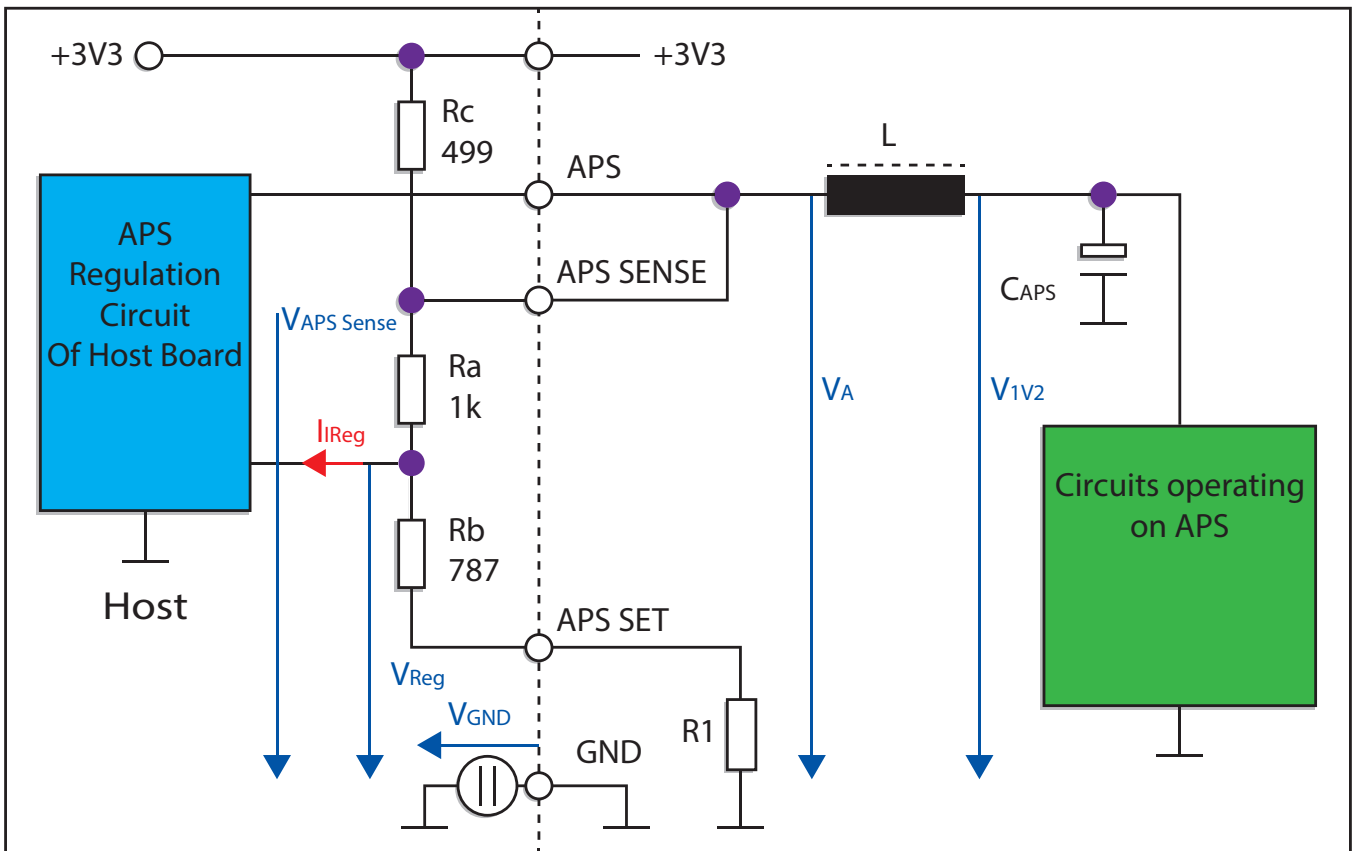
7. Pin Descriptions

Pin	Name	Dir	Logic	Function
1	GND			Electrical Ground
2	GND			Electrical Ground
3	GND			Electrical Ground
4	5.0V			Power
5	3.3V			Power
6	3.3V			Power
7	APS			Adaptive Power Supply
8	APS			Adaptive Power Supply
9	LASI	O	1.2V CMOS Open Drain	Link Alarm Status Interrupt, low active, Open Drain Output A pull-up resistor with 10-22KΩ to 1,2V is expected. Logic High: Normal Operation Logic Low: Link Alarm is indicated
10	Reset	I	1.2V CMOS Open Drain	Low active Reset Input 10KΩ pull-up on Transceiver Logic high = Normal Operation Logic Low = Reset asserted
11	VEND SPECIFIC			Vendor Specific Pin, leave unconnected
12	TX ON/OFF	I	1.2V CMOS Open Drain	High active Transmitter Enable Input 10KΩ pull-up on Transceiver Logic high = Transmitter active (normal operation) And Register Bit 1.9.0 set to low as well Logic Low = shut down of Transmitter
13	RESERVED			RESERVED
14	MOD DETECT	O		1kΩ to Ground On Transceiver
15	VEND SPECIFIC			Vendor Specific Pin, leave unconnected
16	VEND SPECIFIC			Vendor Specific Pin, leave unconnected
17	MDIO	I/O	1.2V CMOS	Management Data I/O. Requires external 10-22 kΩ pullup to 1.2 V on host.
18	MDC	I	1.2V CMOS	Management Clock Input
19	PRTAD4	I		Port Address Bit 4(LOW=0)
20	PRTAD3	I		Port Address Bit 3(LOW=0)
21	PRTAD2	I		Port Address Bit 2(LOW=0)
22	PRTAD1	I		Port Address Bit 1(LOW=0)
23	PRTAD0	I		Port Address Bit 0(LOW=0)
24	VEND SPECIFIC			Vendor Specific Pin,. leave unconnected
25	APS SET	I		Feedback Input for APS, Input of APS Setting Resistor

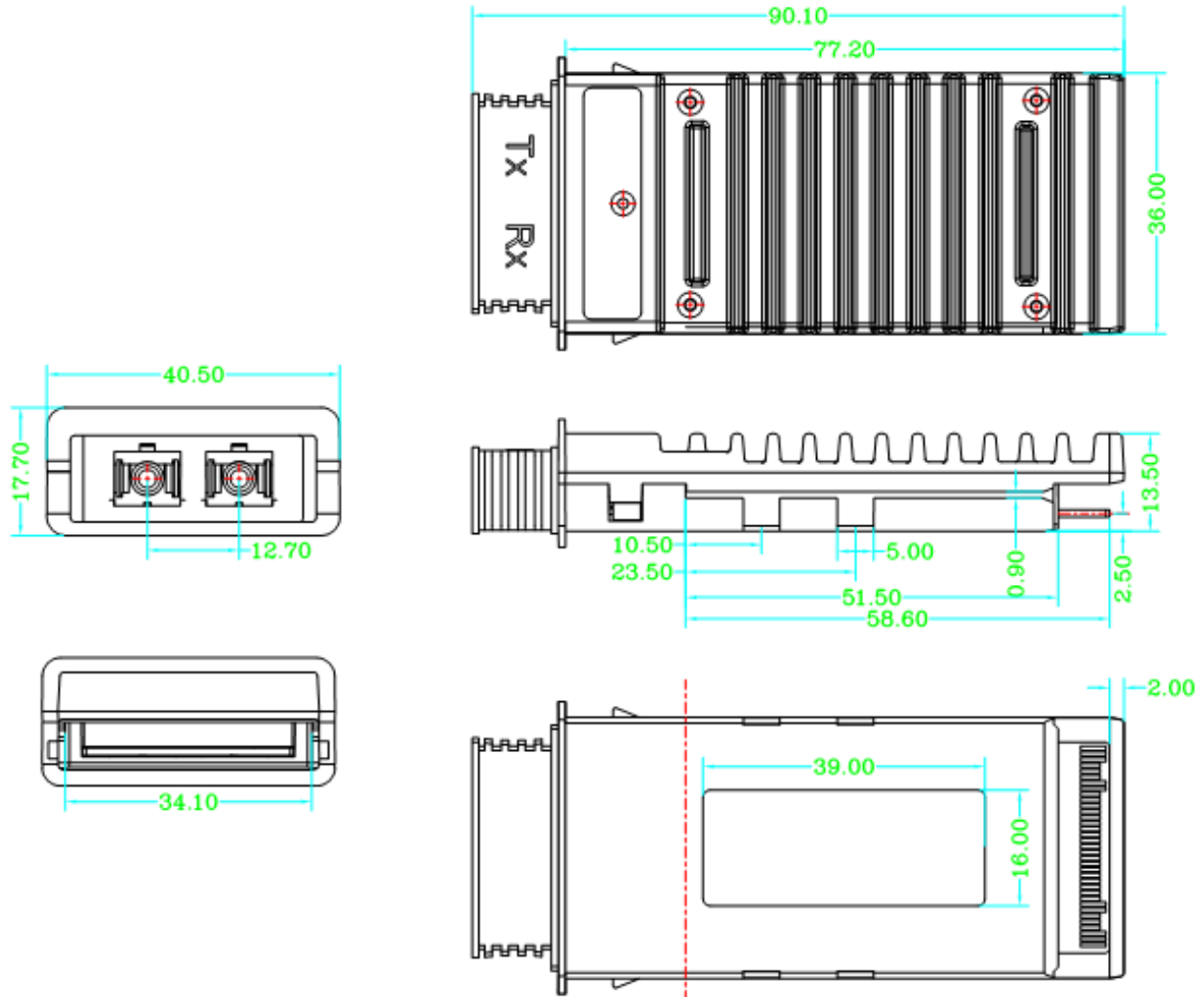
Pin	Name	Dir	Logic	Function
26	RESERVED			RESERVED
27	APS SENSE	O		APS Sense Output for APS Control Circuit
28	APS			Adaptive Power Supply
29	APS			Adaptive Power Supply
30	3.3V			Power
31	3.3V			Power
32	5.0V			Power
33	GND			Electrical Ground
34	GND			Electrical Ground
35	GND			Electrical Ground
36	GND			Electrical Ground
37	GND			Electrical Ground
38	RESERVED			RESERVED
39	RESERVED			RESERVED
40	GND			Electrical Ground
41	RX LANE 0+			Module XAUI Output Lane 0+
42	RX LANE 0-			Module XAUI Output Lane 0-
43	GND			Electrical Ground
44	RX LANE 1+			Module XAUI Output Lane 1+
45	RX LANE 1-			Module XAUI Output Lane 1-
46	GND			Electrical Ground
47	RX LANE 2+			Module XAUI Output Lane 2+
48	RX LANE 2-			Module XAUI Output Lane 2-
49	GND			Electrical Ground
50	RX LANE 3+			Module XAUI Output Lane 2+
51	RX LANE 3-			Module XAUI Output Lane 2-
52	GND			Electrical Ground
53	GND			Electrical Ground
54	GND			Electrical Ground
55	RX LANE 0+			Module XAUI Output Lane 0+
56	RX LANE 0-			Module XAUI Output Lane 0-
57	GND			Electrical Ground
58	TX LANE 1+			Module XAUI Output Lane 1+
59	TX LANE 1-			Module XAUI Output Lane 1-
60	GND			Electrical Ground
61	TX LANE 2+			Module XAUI Output Lane 2+
62	TX LANE 2-			Module XAUI Output Lane 2-

Pin	Name	Dir	Logic	Function
63	GND			Electrical Ground
64	TX LANE 3+			Module XAUI Output Lane 2+
65	TX LANE 3-			Module XAUI Output Lane 2-
66	GND			Electrical Ground
67	RESERVED			RESERVED
68	RESERVED			RESERVED
69	GND			Electrical Ground
70	GND			Electrical Ground

8. Block Diagram of Adapter Power Supply Circuit



9. Package Dimensions



10. Contact Information

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