

**AN-QSFP-LR4**  
40GBASE, QSFP+, LR4 Transceiver

**Features**

- Support up to 11.3Gbps per channel
- QSFP+ MSA compliant
- Compliant with QDR/DDR Infiniband data rates
- Maximum link length of 10km SMF
- Hot pluggable electrical interface
- +3.3V power supply
- Operating case temperature range 0~70°C
- RoHS 6 Compliant
- LC duplex connector
- Maximum power consumptions: 3.5W



**Applications**

- 40GBASE-LR4 40G Ethernet Links
- Infiniband QDR and DDR interconnects
- Client-side 40G Datacom connections

**1. Description**

The Approved Networks QSFP+ LR4 transceiver modules are designed for use in 40 Gigabit Ethernet links over single mode fiber. They are compliant with the QSFP+ MSA and IEEE 802.3ba 40GBASE-LR4. Digital diagnostics functions are available via an I2C interface, as specified by the QSFP+ MSA. The transceiver is RoHS-6 compliant and lead-free per Directive 2011/65/EU, and Application Note AN-2038.

The module supports link lengths of 10KM. It primarily enables high-bandwidth 40G optical links over ribbon fiber cables terminated with multi-fiber connectors, and could also be used along with ribbon to duplex fiber breakout cables for connectivity to four 10GBASE-LR optical interfaces.

## 2. Absolute Maximum Ratings

These values represent the damage threshold of the module. Stress in excess of any of the individual maximum ratings can cause damage to the module even if all other parameters are within recommended Operating conditions.

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	Ts	-40	85	°C
Operating Case Temperature	Top	0	70	°C
Power supply Voltage	Vcc	0	3.6	V
Relative Humidity	RH	0	85	%
Maximum Optical Input Power	Pin	-5	0	dBm

## 3. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Operating Case Temperature	TC	0		+70	°C
Power Supply Voltage	Vcc	3.14	3.3	3.47	V
Power Supply Current	ICC			1000	mA
Power Dissipation	PD			3.5	W
Data Rate per Lane	DR		10.3125	11.3	Gbps
Link Distance on SMF		2		10	km

## 4. Transmitter Specification ( Optical )

Parameter	Symbol	Min	Typ.	Max	Unit
Center wavelength	$\lambda_{c0}$	1264.5		1277.5	nm
	$\lambda_{c1}$	1284.5		1297.5	
	$\lambda_{c2}$	1304.5		1317.5	
	$\lambda_{c3}$	1324.5		1337.5	
Side-mode suppression Ratio	SMSR	30			dB
Extinction Ratio	ER	3.5		4	dB
Spectral Width	$\Delta\lambda$			1	nm
Average launch power	PO,AVG	-7		2.3	dBm
Optical Modulation Amplitude, each lane	OMA	-4		+3.5	dBm
Relative Intensity Noise	Rin			-128	dB/Hz
Optical Return Loss Tolerance 20 dB					
Transmitter Reflectance	RT			-12	dB
Transmitter Eye Mask Definition (X1,X2,X3, Y1, Y2, Y3)		Compliant with 802.3ba Standard (0.25,0.4,0.45,0.25,0.28,0.4)			
Average Launch Power OFF	POFF			-30	dBm

## 5. Transmitter Specification ( Electrical )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V <sub>cc</sub>	3.14	3.3	3.47	V
Supply Current	I <sub>cc</sub>			1000	mA
Maximum Power Consumption				3.5	W
Data Rate per lane			10.3125	11.3	Gb/s
Differential Input Impedance			100		ohms

## 6. Receiver Specification ( Optical )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Center wavelength	$\lambda_{c0}$	1264.5		1277.5	nm
	$\lambda_{c1}$	1284.5		1297.5	
	$\lambda_{c2}$	1304.5		1317.5	
	$\lambda_{c3}$	1324.5		1337.5	
Damage Threshold				3.3	dBm
Receiver Reflectance				-26	dB
Receiver Sensitivity (OMA) per lane				-11.5	dBm
Stressed Receiver Sensitivity (OMA), each lane				-9.6	dBm
LOS Assert	LOS	-30			dBm
LOS De-assert	LOSD			-17	dBm
LOS Hysteresis	LOSH	0.5			dBm

## 7. Receiver Specification ( Electrical )

Parameter	Symbol	Min.	Typ.	Max.	Unit
Differential Data Output Voltage Swing	V <sub>out, p-p</sub>	200		850	mV
Output Differential Impedance	R <sub>out</sub>		100		$\Omega$

## 8. Pin Definitions

The QSFP+ modules are hot-pluggable. Hot pluggable refers to plugging in or unplugging a module while the host board is powered. The QSFP+ hot connector is a 0.8mm pitch 38 position right angle improved connector specified by SFF-8436, or stacked connector with equivalent electrical performance. Host PCB contact assignment is shown in Figure 1 and contact definitions are given in Table below.

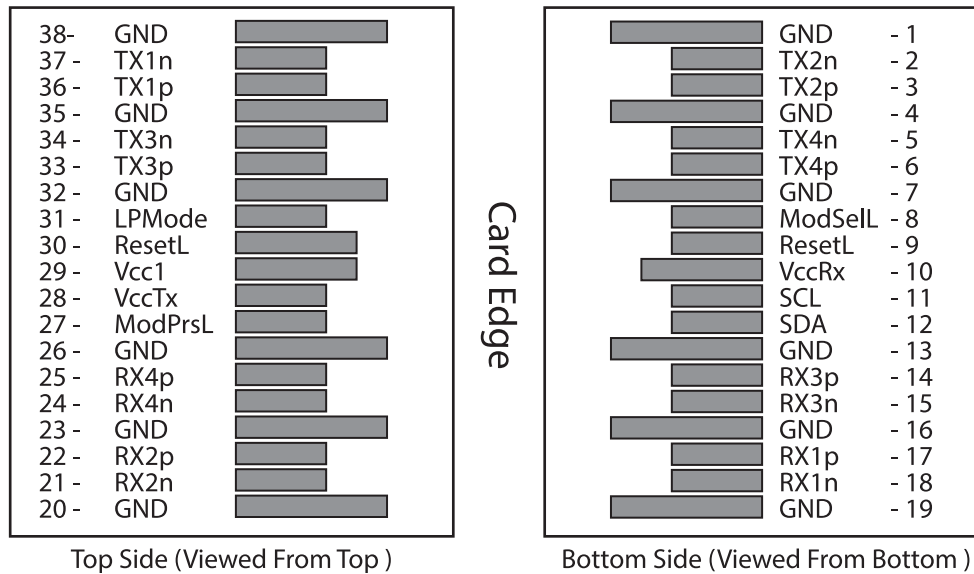


Figure 1. Interface to Host PCB

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground
2	CML-I	Tx2n	CH2 Transmitter Inverted Data Input
3	CML-I	Tx2p	CH2 Transmitter Non-inverted Data Input
4		GND	Module Ground
5	CML-I	Tx4n	CH4 Transmitter Inverted Data Input
6	CML-I	Tx4p	CH4 Transmitter Non-inverted Data Input
7		GND	Module Ground
8	LVTTL-I	ModSelL	Module Select
9	LVTTL-I	ResetL	Module Reset
10		VccRX	+3.3V Power Supply Receiver
11	LVC MOS-I/O	SCL	2-wire serial interface clock
12	LVC MOS-I/O	SDA	2-wire serial interface data
13		GND	Module Ground
14	CML-O	Rx3p	CH3 Receiver Non-inverted Data Input
15	CML-O	Rx3n	CH3 Receiver Inverted Data Input
16		GND	Module Ground
17	CML-O	Rx1p	CH1 Receiver Non-inverted Data Input

# AN-QSFP-LR4

40GBASE, QSFP+, LR4, (SM)

1264.5 NM - 1337.5 NM, 10 KM REACH, LC

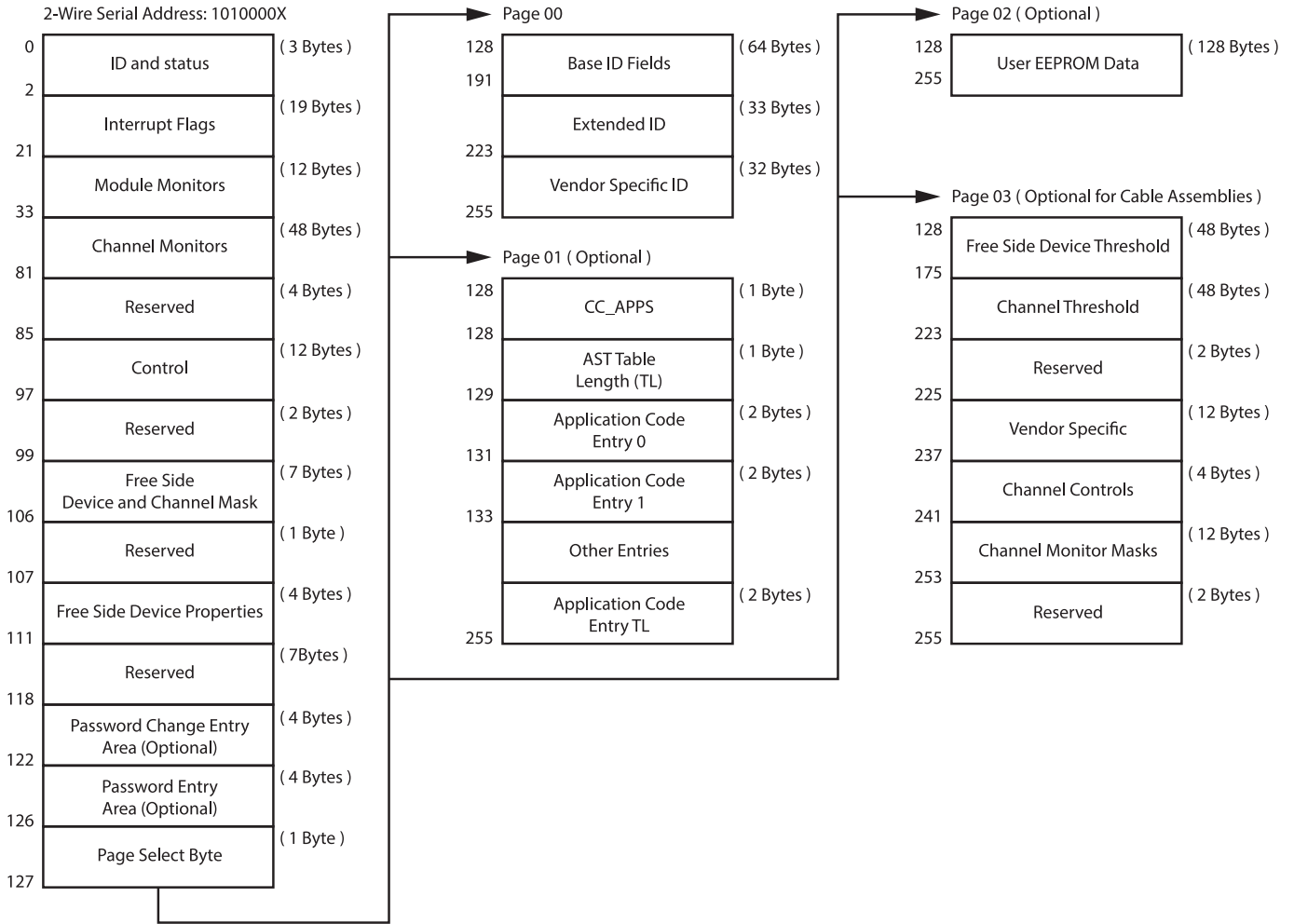
Pin	Logic	Symbol	Name/Description
18	CML-O	Rx1n	CH1 Receiver Inverted Data Input
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	Rx2n	CH2 Receiver Inverted Data Input
22	CML-O	Rx2p	CH2 Receiver Non-inverted Data Input
23		GND	Module Ground
24	CML-O	Rx4n	CH4 Receiver Inverted Data Input
25	CML-O	Rx4p	CH4 Receiver Non-inverted Data Input
26		GND	Module Ground
27	LVTTL-O	ModPrsL	Module Present
28	LVTTL-O	IntL	Interrupt
29		VccTX	+3.3V Power Supply Transmitter
30		Vcc1	+3.3V Power Supply
31	LVTTL-I	LPMODE	Low Power Mode
32		GND	Module Ground
33	CML-I	Tx3p	CH3 Transmitter Non-inverted Data Input
34	CML-I	Tx3n	CH3 Transmitter Inverted Data Input
35		GND	Module Ground
36	CML-I	Tx1p	CH1 Transmitter Non-inverted Data Input
37	CML-I	Tx1n	CH1 Transmitter Inverted Data Input
38		GND	Module Ground

## Notes:

1. Module circuit ground is isolated from module chassis ground within the module
2. Open collector, should be pulled up with 4.7K-10K ohms on the host board to a voltage between 3.15V and 3.6V.

## 9. 2-wire Management Interface

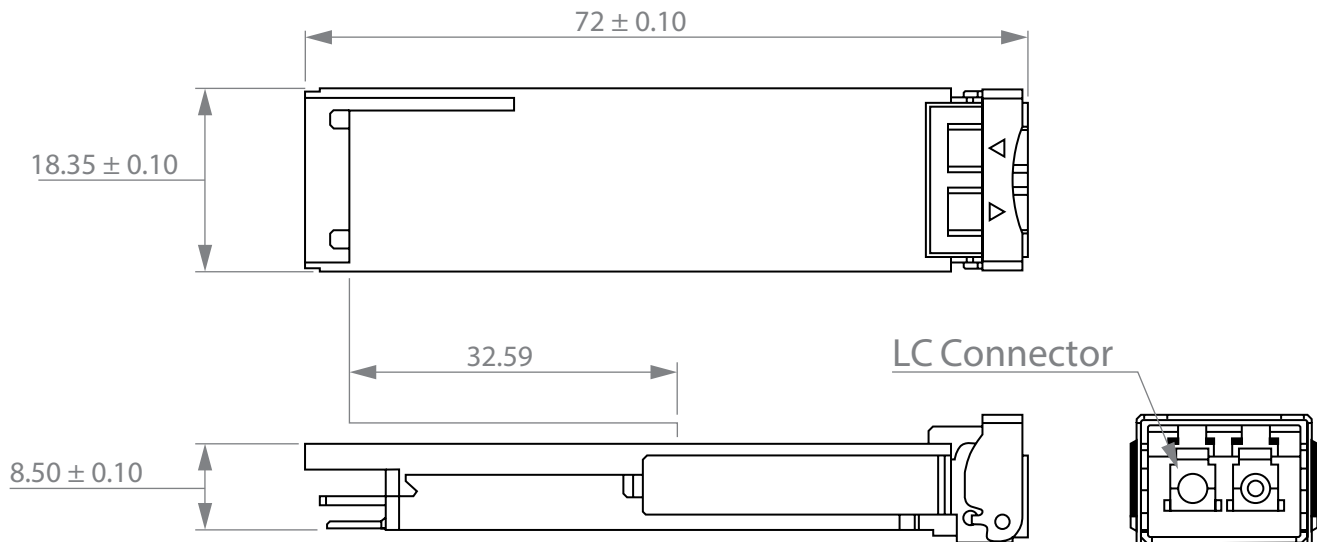
The transceivers provide management two-wire interface and the management memory map is specified by SFF-8436.



## 10. ESD

This module high speed pins withstand 1KV electrostatic discharge on Human Body Model per JESD22-A114. The exception of high speed pins withstand 2KV electrostatic discharge based on Human Body Model per JESD 22-A114. The QSFP+ module meet ESD requirement in EN61000-4-2, criterion B test specification. The transceiver is shipped in ESD protective packaging. It should be removed from the packaging and handled only in an ESD protected environment.

## 11. Package Dimentions ( Unit: MM )



## 12. Contact Information

Approved Networks is a leading supplier of Network Transceivers and Connectivity products to Channel Partners, Resellers, and OEMs. With more than 9 years of direct industry experience, our products are resident in the most demanding and mission critical functional networks Worldwide. We serve as a Master Distributor to the largest CMs in the world and deploy the most rigorous testing and firmware management programs to bring the highest level of functional product to the market at a cost that makes sense.

Corporate Offices: **Approved Networks, Inc.**

Tel: 800.590.9535

Web: <http://www.approvednetworks.com>